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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/719,912	11/21/2003	Tzong Da Ho	55855-DIV (71987)	4010

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EXAMINER	
DUONG, KHANH B	
ART UNIT	PAPER NUMBER
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/719,912	HO ET AL.	
	Examiner	Art Unit	
	Khanh B. Duong	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the request for reconsideration filed on July 26, 2007.

Accordingly, no claim was amended or canceled.

Currently, claims 1-4 remain pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kasem et al. (U.S. Patent No. 6,392,290) in view of Kenichi (JP 406349983 A) and Noquil et al. (U.S. Patent No. 6,645,791).

Kasem et al. ("Kasem") discloses in FIGs. 47A-58C [see col. 9, line 24 to col. 10, line 55] a method for fabricating a thermally-enhanced wafer-level chip scale package, comprising the steps:

(1) preparing a semiconductor wafer 227 having a front side and a back side, and which is predefined into a plurality of integrated circuit chips 220 [see FIG. 47A-47C];

(2) performing a bumping process to bond a plurality of solder bumps 248 on the front side of the semiconductor wafer 227 [see FIG. 56A-56C];

(3) performing a back-side lapping process to grind away a back-side portion of the semiconductor wafer 227 [see FIG. 54A-54C];

(4) attaching a thermally-conductive stiffener (Cu heat sink) 245 to the back side of the semiconductor wafer 227 by means of a thermally-conductive adhesive layer 246, wherein the thermally-conductive stiffener 245 is free of electrical connection with the semiconductor wafer 227 [see FIG. 55A-55C];

(5) performing a singulation process to cut the thermally-conductive stiffener 245 and cut apart each chip 220 from the semiconductor wafer 227 [see FIG. 58A-58C]; and

(6) performing a flip-chip die bonding process to mount each singulated chip 220 by means of the solder bumps 248 onto a circuited substrate [see FIG. 58A-58C].

Re claim 1, Kasem does not disclose performing the singulation process along a straight line such that the thermally-conductive stiffener and the semiconductor wafer are cut together. In addition, Kasem discloses performing the bumping process after, instead of prior to, the back-side lapping process.

Kenichi shows in figures 1-2 performing the singulation process along a straight line 11 such that a thermally-conductive stiffener 10 and a semiconductor wafer 8 are cut together for the expressed purposes of maximizing process efficiency and reducing manufacturing costs [see attached English abstract and translations]. However, Kenichi is silent in regard to performing a bumping process after a back-side lapping process.

Noquil et al. ("Noquil") shows in FIG. 3 performing a bumping process after a back-side lapping process [see col. 5, line 59 to col. 6, line 2].

Since Kasem, Kenichi and Noquil are from the same field of endeavor, the purposes disclosed by Kenichi and Noquil would have been recognized in the pertinent prior art of Kasem.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the method disclosed by Kasem as suggested by Kenichi because of the desirability to maximize process efficiency and reduce manufacturing costs. Furthermore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the method disclosed by Kasem as suggested by Noquil because the selection of any order/sequence of performing process steps is prima facie obvious in the absence of new or unexpected results. See *Ex parte Rubin*, 128 USPQ 440 (Bd. App. 1959); *In re*

Burhans, 154 F. 2d 690, 69 USPQ 330 (CCPA 1946); and *In re Gibson*, 39 F.2d 975, 5 USPQ 230 (CCPA 1930).

Re claim 3, Kasem discloses the thermally-conductive stiffener (heat sink) 245 is made of copper [see col. 10, lines 22-26].

Re claim 4, Kasem does not disclose the thermally-conductive stiffener 245 being made of copper alloy.

Kenichi teaches in a thermally-conductive stiffener (heat sink) 3 comprising copper alloy has excellent thermal conductivity [see attached English translation, page 1, paragraph 0011].

Since Kasem and Kenichi are from the same field of endeavor, the purpose disclosed by Kenichi would have been recognized in the pertinent prior art of Kasem.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the method disclosed by Kasem as suggested by Kenichi because such conductive material is selected so that it acts as a heat sink which increases the thermal performance of the chip package.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kasem, Kenichi and Noquil, as applied to claims 1, 3 and 4 above, and further in view of Chen et al. (U.S. Patent No. 6,403,882).

Re claim 2, Kasem discloses the thermally-conductive adhesive 246 comprises solder or epoxy, but does not disclose the epoxy comprising silver epoxy. Kenichi and Noquil are silent in regard to the material of a thermally-conductive adhesive.

Chen et al. ("Chen") suggests attaching a thermally-conductive stiffener 50 comprising of copper to the back side of a semiconductor wafer 20 by a conductive adhesive 45 comprising silver epoxy [see col. 2, lines 45-48; and col. 3, lines 15-25].

Since Kasem, Kenichi, Noquil and Chen are from the same field of endeavor, the purpose disclosed by Chen would have been recognized in the pertinent prior art of Kasem, Kenichi and Noquil.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combined method disclosed by Kasem, Kenichi and Noquil as suggested by Chen because Chen states that the conductive adhesive 45 is selected so that it remains stable during subsequent processing of the chip package at elevated temperatures [see Chen: col. 3, lines 6-14, and lines 45-52].

Response to Arguments

Applicant's arguments filed July 26, 2007 have been fully considered but they are not persuasive.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Applicant persistently argues that the proposed combination of Kasem in view of Kenichi and Noquil does not teach or suggest attaching a thermally-conductive stiffener to the back side of a semiconductor wafer, and then performing a singulation process to

cut apart each chip from the semiconductor wafer. In response, the Examiner respectfully disagrees because Kenichi clearly shows in figures 1-2 performing the singulation process along a straight line 11 such that a thermally-conductive stiffener 10 and a semiconductor wafer 8 are cut together [see attached English abstract and translations]. Note that Kenichi clearly shows attaching the thermally-conductive stiffener (or heat dissipating plate) 10 to the back side of a semiconductor wafer 8 prior to cutting apart each chip from the semiconductor wafer 8. Furthermore, it is respectfully submitted that the heat sink 10 of Kenichi, while providing a heat-dissipating function, also functions as a stiffener which protects singulated chips against cracking or chipping during subsequent processing steps.

Applicant further argues that Noquil does not teach performing a back-side lapping process after performing a bumping process. In response, the Examiner respectfully disagrees because Noquil clearly teaches performing a back-side lapping process after performing a bumping process (soldering with a solder mask 200) [see col. 5, lines 59-63].

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh B. Duong whose telephone number is (571) 272-1836. The examiner can normally be reached on Monday to Friday from 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith, can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KBD

Zandra V. Smith
Supervisory Patent Examiner
10 Oct. 2007